AND8176/D

Applications for the NE521/522

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APPLICATION NOTE

Comparators

Voltage comparators are high gain differential input-logic output devices. They are specifically designed for open-loop operation with a minimum of delay time. Although variations of the comparator are used in a host of applications, all uses depend upon the basic transfer function. Device operation is simply a change of output voltage dependent upon whether the signal input is above or below the threshold input.

Comparator inputs are customarily marked with plus or minus signs to indicate their polarity. For example, the circuit of Figure 1 produces a logic 1 level when the non-inverting input is more positive than the reference voltage.

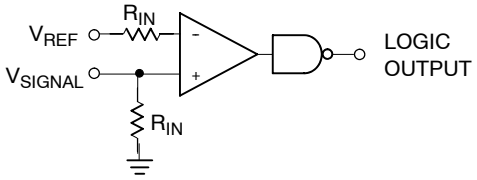

Figure 1. Basic Comparator Circuit

Definitions

Many similarities exist between operational amplifiers and the amplifier section of voltage comparators. In fact, op amps can be used to implement the comparator function at low frequencies.

Thus, the characteristic definitions presented here are similar to those reviewed for op amps.

Input Offset Voltage

As with operational amplifiers, the non-ideal comparator possesses some offset voltage. The definition differs slightly in that the output structure of comparators is digital rather than linear. Hence, input offset voltage is defined for comparators as the DC voltage required at the input to force the output to the logic threshold of ensuing devices (1.2 V for TTL).

Input Offset Current

Imbalances of input bias current arise from small variances of the junction geometry of the differential input amplifier. As for op amps, the imbalance is referred to as input offset current.

Bias Current

As with op amps the input structure of comparators is usually a differential bipolar stage. Input bias current is the average of the two input currents.

Common-Mode Range

When specifying voltage comparators, one of the key parameters is common-mode range, which is defined as the range of voltages over which both inputs can be varied simultaneously without abnormal output voltage transitions or device degradation. This parameter must be kept uppermost in the designer's mind because the reference and signal voltages become common-mode signals at threshold. All ranges of input signals thus must be within the common-mode range of the input amplifier.

Voltage Gain

Specifications of voltage gain refer to the overall gain of the device, the bulk of which occurs in the amplifier section.

In general, higher gains would be advantageous for resolving smaller input signals. Of course, the propagation delay suffers due to the more severe saturation of the transistors. Typical gains for TTL output devices are set for 5000 V/V. This gain provides 5.0 V of output swing with 1.0 mV input signal change for reasonable accuracy, but does not contribute severely to the overload recovery delay.

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Propagation Delay

Voltage comparisons of analog signals with a reference voltage usually require that the operation take as little time as possible. Long delays in the comparator cause a pulse position error at the output since the analog signal in the meantime has changed value. At low frequencies the delay is of small consequence, but at higher frequencies, transit time becomes intolerable. Design of voltage comparator devices includes, as a prime goal, the minimizing of transit times.

Propagation delay testing is done under worst−case conditions. The recovery from saturation varies, depending upon the initial state of the amplifier and the overdrive. Worst−case conditions begin by applying a 100 mV signal on the reference terminal. With no signal applied, the amplifier is in saturation in one direction. A step input pulse on the signal line of 100 mV $\pm V_{OS}$ will bring the amplifier to a threshold level. Propagation delay at this point is undefined since the output has not switched.

To attain output switching, a small overdrive is necessary. Propagation delay is tested in a configuration such as Figure 2. The input is a step function of 100 mV plus a specified excess or overdrive signal. This causes the amplifier to be exercised from saturation in one direction to saturation in the other for worst−case propagation delay. Note that larger overdrive reduces delay time as can be seen in Figure 3. An overdrive of 5 mV causes 12 ns delay, whereas a 100 mV overdrive improves transit time to only 6 ns.

If the measurement were made without initial saturation (less than 100 mV/V threshold) the delay time would be less, due to the decreased storage times of unsaturated transistors.

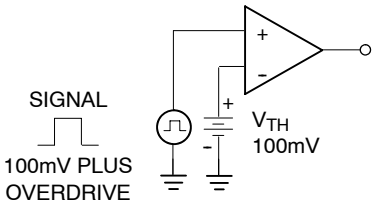


Figure 2. Propagation Delay Test Setup

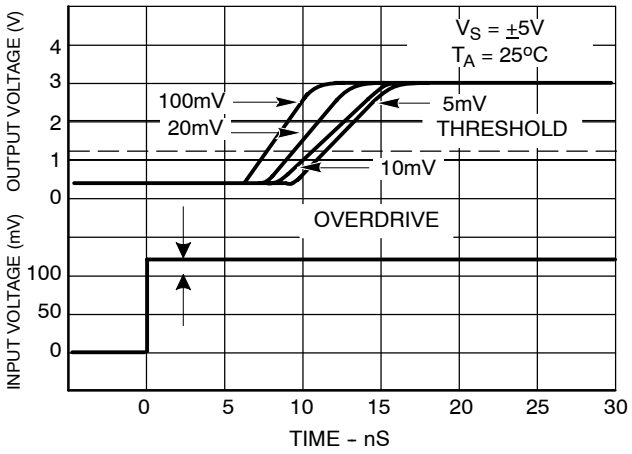


Figure 3. Response Time for NE521 Comparator for Various Input Overdrives

State−of−the−Art

Comparator design has always been optimized for four basic parameters. They are:

1. High Speed
2. Wide Input Voltage Range
3. Low Input Current
4. Good Resolution

Unfortunately, these four parameters are not compatible. For instance, gain and input current can be improved by using thinner diffusions for higher beta, but only at the expense of input voltage range. Higher gain also means higher saturation for an increase in delay time. So it becomes obvious that older comparators such as the 710 were designed with the best compromises in mind using standard processing.

One method of improving overall response adds gold doping to the processing flow. The gold dopant causes a decrease in minority carrier lifetime which aids the recombination process and shortens the saturation recovery time. Unfortunately, the transistor beta is adversely affected by gold, causing slightly higher bias and offset currents.

It was not until the advent of the Schottky clamp that a vast improvement in speed without input degradation was possible. A very familiar term in the semiconductor industry, the Schottky Barrier Diode's (SBD) location is illustrated in Figure 4.

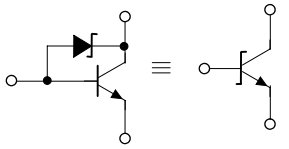


Figure 4. Schottky Clamped Transistor

The Schottky clamped transistor is formed by paralleling the Schottky diode with the base-collector junction of the NPN transistor. Without the clamp, as base drive is increased the collector voltage falls until hard saturation occurs. At this point the collector voltage is very near the emitter voltage, and stored charges in the junctions causes slow recovery from saturation after base drive has been removed. The forward voltage drop of the Schottky diode is 0.4 V-less than the forward drop of silicon diodes. This difference in forward drop is used by placing the diode across the transistor base-collector junction.

The Schottky diode becomes forward-biased when the collector voltage falls 0.4 V below the base voltage. Excess base drive is then shunted into the collector circuit, prohibiting the transistor from reaching classic saturation. With almost no stored charge in either the SBD or the transistor, there is a large reduction in storage time. Thus, transistor switching time is significantly reduced.

A cross sectional area of the Schottky diode is shown in Figure 5.

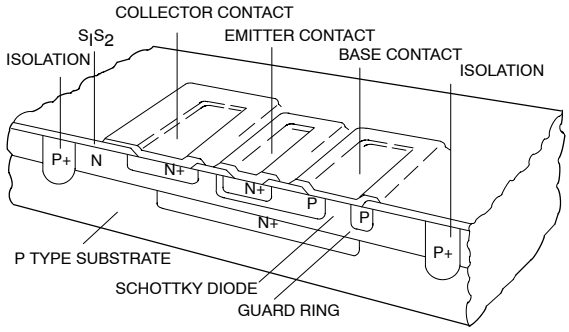


Figure 5. Schottky Clamped Transistor Geometry

Comparing the Comparators

Presently available comparator ICs range from the ultra fast SE/NE521 to the general purpose comparator fashioned from an inexpensive op amp. Selection of the device depends upon the application in which it will be used. Speed of conversion is often of primary importance to minimize pulse position errors of high frequency signals. At other times the requirements are much less stringent, allowing the use of a general purpose comparator. A handy reference guide to the major parameters is summarized in Table 1. The necessary parameters can be chosen to select the proper device.

A general description of the comparator devices is included here to familiarize the user with available devices and their advantages.

NE521/522 Comparators

Processed with state-of-the-art Schottky barrier diodes, the NE521/522 series devices provide good input characteristics while providing the fastest analog-to-TTL conversion. Total delay from input to output is typically 6 ns with a guaranteed speed of 12 ns. Additional features of this device include the dual configuration and individual output strobes to simplify system logic. The NE522, although sacrificing some speed, features open-collector outputs for party line or wired-OR configurations for additional system flexibility.

Table 1. Comparator Selection Guide (Parameters are based on min/max limits at 25°C as defined in the individual data sheet.)

Device	Prop Delay (ns)	V_{OS} (mV)	I_{OS} (μA)	I_{BIAS} (μA)	Gain	CMR (V)	Benefits
NE521	12	7.5	5	20	5000	±3	Dual, very fast, standard supplies TTL compatible, individual and common strobe.
NE522	15	7.5	5	20	5000	±3	Same as NE521 plus open-collector outputs for additional decoding.
LM311	200	7.5	0.05	0.25	200 k	V+ - 1.5 V	High common-mode input range, +5 V to ±15 V supply, strobe input, open-collector output.
LM319	80	8	0.2	1.2	40 k	±5	Low input bias, dual, +5 V to ±15 V supply, open-collector output.
LM333	1300	2	0.05	0.25	200 k	V+ - 1.5 V	Low input bias, dual, +5 V to ±15 V supply, open-collector output.
LM393	1300	2	0.05	0.25	200 k	V+ - 1.5 V	Same as LM339 but dual.

Applications

High−speed comparators are capable of making logic decisions in less than 10ns. They are easily applied and possess good input and power supply noise rejection. As with all linear ICs, however, some preliminary steps should be taken in their use.

General Precautions

Layout

The comparator is capable of resolving sub−millivolt signals. To prevent unwanted signals from appearing at signal ports, good physical layout is required. For any high−speed design, ground planes should be used to guard against ground loops and other sources of spurious signals. At high frequencies, hidden signal paths become dominant. Distributed capacitance is a particular nuisance. If care is not taken to isolate output from input, distributed capacitance can couple a few millivolts into the input, causing oscillation.

Another source of spurious signals is ground current. Input structures are relatively high impedance while the gate structures of comparators run with large signal and ground currents. If this gate ground current is allowed to pass near the input signal path, the small impedances of the ground circuit will cause millivolt changes in reference or signal voltages producing errors, sustained oscillation, ringing, or excessive V_{OS}. A ground plane arranged such that output currents do not flow near input areas is highly recommended.

Power Supplies

Another general precaution that should always be exercised is power supply bypassing. As mentioned, the name of the game is speed. Very high−speed gates are used to produce the desired output logic levels. Maximizing response speed also requires higher current levels, giving rise to power supply noise. For this reason, good power supply bypassing very close to the device itself is always mandatory. A tantalum capacitor of 1 to 10 μF in parallel with 500 to 1000 pF will prove effective in most cases. Lead lengths should be as short as physically possible to preserve low impedances at high frequency.

Unused Inputs

Some currently available comparators such as the NE521 and NE522 are dual devices. Most often both sections of these devices will be utilized. Should a system utilize one device, the unused inputs should be biased in a known condition. The high gain−bandwidth may otherwise cause oscillations in the unused comparator section. A low impedance should be provided from both unused inputs to ground. A resistor of relatively high impedance may then be used to supply a differential input on the order of 100 mV to insure the comparator assumes a known state.

If the inverting input is tied to the positive differential voltage the gate output will be low. The strobe inputs then provide a means of utilizing the Schottky gate for other system logic functions.

If the strobe inputs are not used, they should be connected to the output of a logic gate that is always high, or to the +5 V supply through a 5 to 10 kΩ resistor. They should never be tied directly to the +5 V supply as the relatively minor spiking on the supply may damage these inputs.

Common−Mode Signals

Manufacturers specify the maximum voltage range over which the inputs may be taken. In addition, the maximum differential voltage that may be safely applied to the inputs is specified. In the case of the NE521 comparator, the differential voltage is restricted to less than ±6 V, with a common−mode of ±5 V. That these two quantities interact cannot be overlooked. For instance, with both inputs at ±4 V the common−mode restriction is satisfied. If V_{REF} is now left at +4 V the signal input may not be taken more than 2 V below ground because the differential signal becomes 6 V.

It is important to observe this maximum rating since exceeding the differential input voltage limit and drawing excessive current in breaking down the emitter−base junctions of the input transistors could cause gross degradation in the input offset current and bias current parameters.

It is also important to note that response time is specified for a common−mode voltage of zero and may degrade when the common−mode voltage approaches the common−mode specification limits.

Exceeding the absolute maximum positive input voltage limit of the device will saturate the input transistor and possibly cause damage through excessive current. However, even if the current is limited to a reasonable value so that the device is not damaged, erratic operation can result.

Input Impedance

The differential bias and offset currents of comparators are minimized by design. As was pointed out for op amps, the input resistance seen by both inputs should be equal. This reduces to a minimum the contribution of offset current to threshold error. Unbalanced input impedance also adds to the offset error due to the difference in voltage drop across the input resistances.

Basic Applications

The basic comparator circuit and its transfer function were presented by Figure 1.

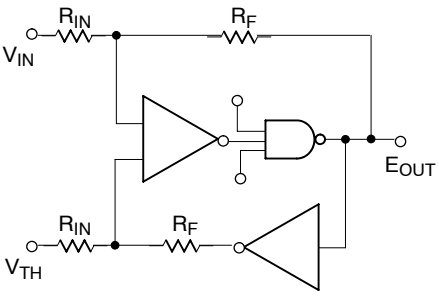
When the input exceeds the reference voltage, the output switches either positive or negative, depending on how the inputs are connected.

The vast majority of specific applications involve only the basic configuration with a change of reference voltage. A to D converters are realized by applying the signal to one terminal and the voltage derived from a ladder network to the other. Limit detectors are likewise made from only the very basic circuit. Both are only a small deviation from the basic level detector.

Hysteresis

Normally saturated high or low, the amplifiers used in voltage comparators are seldom held in their threshold region.

They possess high gain-bandwidth products and are not compensated to preserve switching speed. Therefore, if the compared voltages remain at or near the threshold for long periods of time, the comparator may oscillate or respond to noise pulses. For instance, this is a common problem with successive approximation D to A converters where the differential voltage seen by the comparator becomes successively smaller until noise signals cause indecision. To avoid this oscillation in the linear range, hysteresis can be employed from output to input. Figure 6 defines the arrangement. Both positive and negative feedback is provided by R_{IN} and R_F.



NOTE:

$$V_{HYST} = \frac{E_{OUT} \cdot R_{IN}}{R_{IN} + R_F}$$

Figure 6. Level Detector With Hysteresis

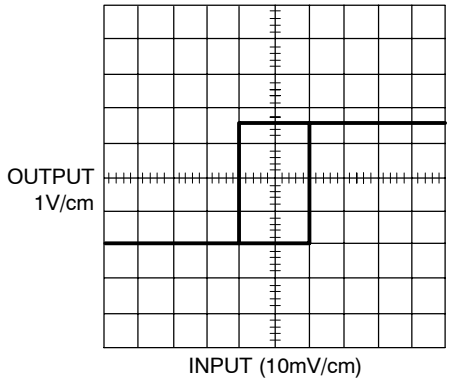


Figure 7. 0 V Level Detector With ±10 mV Hysteresis

Hysteresis occurs because a small portion of the "one" level output voltage is fed back in phase and added to the input signal. This feedback aids the signal in crossing the threshold. When the signal returns to the threshold, the positive feedback must be overcome by the signal before switching can occur. The switching process is then assured and oscillations cannot occur. The threshold "dead zone" created by this method, illustrated in Figure 7, prevents output chatter with signals having slow and erratic zero crossings.

As shown in Figure 6, the voltage feedback is calculated from the expression:

$$V_{HYST} = \frac{E_{OUT} \cdot R_{IN}}{R_{IN} + R_F}$$

where E_{OUT} is the gate high output voltage.

The hysteresis voltage is bounded by the common-mode range and the ability of the gate to source the current required by the feedback network. If symmetrical hysteresis is desired, an additional inverting gate is required if the comparator does not have differential outputs. The NE521 and NE522 devices will require the inverter. Care should be taken in the selection of the inverter that propagation delay is minimum, especially for very high-speed comparators such as the NE521.

Line Receiver

Retrieving signals which have been transmitted over long cables in the presence of high electrical noise is a perfect application for differential comparators. Such systems as automated production lines and large computer systems must transmit high frequency digital signals over long distances.

If the twisted-pair of the system is driven differentially from ground, the signals can be reclaimed easily via a differential line receiver.

Since the electrical noise imposed upon a pair of wires takes the form of a common-mode signal, the very high common-mode rejection of the NE521/522 makes the unit ideal for differential line receivers. Figure 8 depicts the simple schematic arrangement. The NE521 is used as a differential amplifier having a logic level output. Because common-mode signals are rejected, noise on the cable disappears and only the desired differential signal remains. Figure 9 illustrates the NE521 response to the 200 mV_{P-P} 10 MHz differential signal. In Figure 10 the same signal has been buried in 5 V_{P-P} of 1 MHz common-mode "noise."

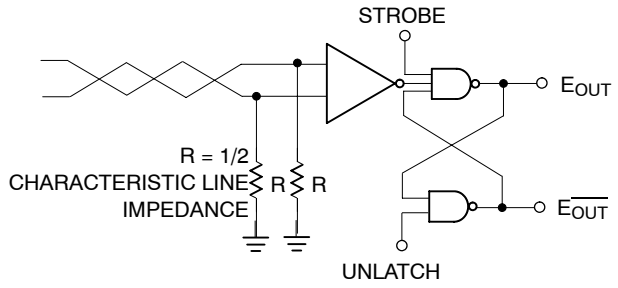


Figure 8. Line Receiver

The circuit suffers no degradation of signal. If desired, several NE522 comparators may be “wire-ORed,” or a latched output can be built as shown in Figure 8.

The NE521 comparator has the advantage of wider bandwidth to permit higher data rates.

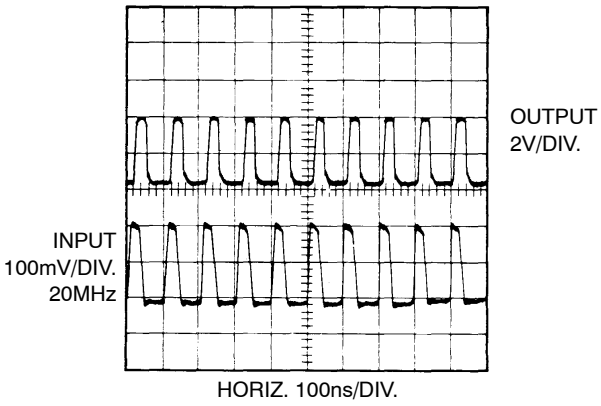


Figure 9. Line Receiver Response

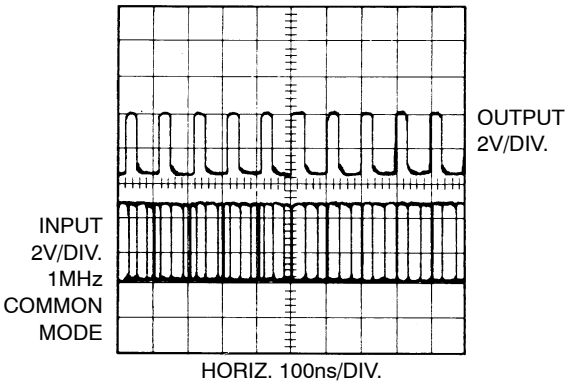


Figure 10. Response During Common-Mode Noise

Double-Ended Limit (Window) Detector

Many system designs require that it be known when a signal level lies between two limits. This function is easily accomplished with a single NE522 package. The schematic and transfer curve of the circuit is shown in Figure 11.

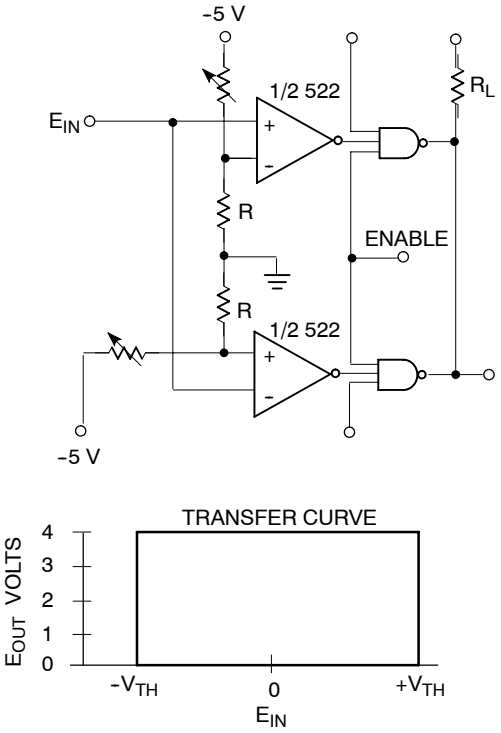


Figure 11. Double-Ended Limit Detector

Each half of the NE522 is referenced to the desired upper or lower voltage limit producing the desired transfer curve shown. Taking advantage of the dual configuration and the open-collectors of the NE522 minimizes external components and connections.

Crystal Oscillator

Any device with a reasonable gain can be made to oscillate by applying positive feedback in controlled amounts. The NE521 will lend itself to crystal control easily, provided the crystal is used in its fundamental mode. Figure 12 shows a typical oscillator circuit.

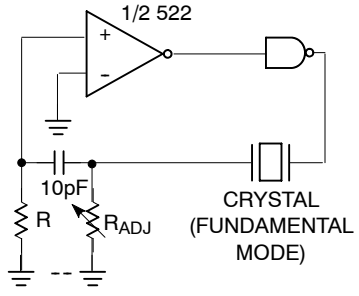


Figure 12. Crystal Oscillator

The crystal is operated in its series-resonant mode, providing the necessary feedback through the capacitor to the input of the NE521. The resistor R_{ADJ} is used to control the amount of feedback for symmetry. Oscillations will start whenever a circuit disturbance such as turning on the power supplies occurs. The NE521 will oscillate up to 70 MHz.

However, crystals with frequencies higher than about 20 MHz are usually operated in one of their overtones. To build an oscillator for a specific overtone requires tuned circuits in addition to the crystal to provide the necessary mode suppression. If the spurious modes are not tuned out, the crystal will oscillate at the fundamental frequency. Higher frequency oscillators could be realized using input and output mode suppression or tuning. The NE522 is especially desirable since the open−collector topology allows the output to be collector−tuned readily.

Analog−to−Digital Converter

There are many types of A to D converter designs, each having its own merits. However, where speed of conversion is of prime interest, the multi−threshold conversion type is used exclusively. It is apparent from Figure 13 that the conversion speed of this design is the sum of the delay through the comparator and the decoding gates.

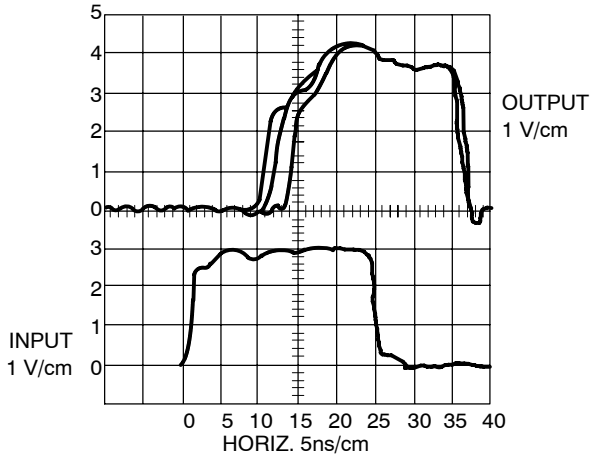


Figure 13. Parallel A to D Response

The sacrifices which must be made to obtain speed are the number of components, bit accuracy and cost. The number of comparators needed for an N−bit converter is 2n−1. Although the NE521 provides two comparators per package, the length of parallel converters is usually limited to less than 4 bits. Accuracy of multi−threshold A to D converters also suffers since the integrity of each bit is dependent upon comparator threshold accuracy.

The implementation of a 3−bit parallel A to D converter is shown in Figure 14 with a 3−bit digital equivalent of an analog input shown in Figure 13.

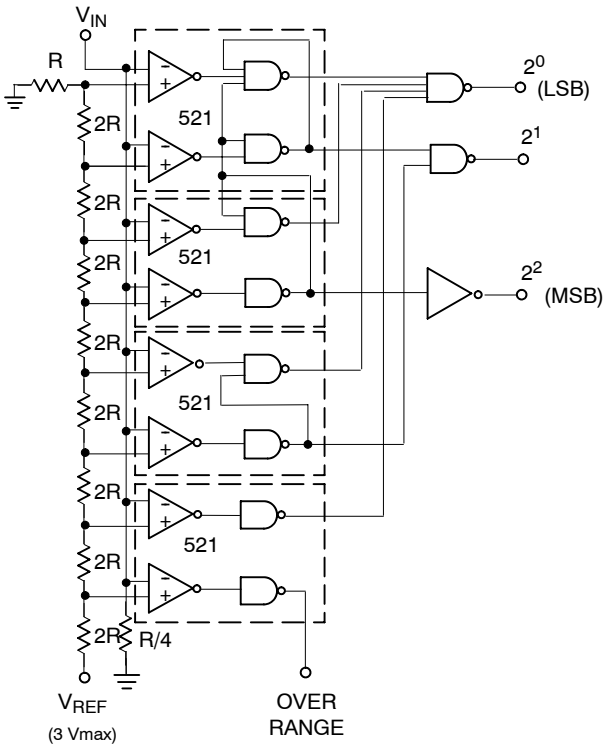


Figure 14. 3−Bit Parallel A to D Converter

Reference voltages for each bit are developed from a precision resistor ladder network. Values of R and 2R are chosen so that the threshold is one half of the least significant bit. This assures maximum accuracy of ± bit.

It is apparent from the schematic that the individual strobe line and duality features of the NE521 have greatly reduced the cost and complexity of the design. The speed of the converter is graphically illustrated by the photo of Figure 13. All 3−bit outputs have settled and are true a mere 15 ns after the input step of 3V has arrived. The output is usually strobed into a register only after a certain time has elapsed to insure that all data has arrived.

Sense Amplifiers

Closely related to the comparator is the sense amplifier. Signals derived from the many sources, such as transducers, are not of sufficient amplitude to be compatible with subsequent logic. It then becomes necessary to amplify and convert the signal to TTL levels, which is the responsibility of the sense amplifier.

Some transducers produce an output current. It remains, then, for the user to convert these currents to TTL levels. A terminating resistor from the drain to ground provides a voltage output proportional to the current and the resistor size. Larger signals can be produced by larger resistors; but in practice, resistors larger than 1kΩ are avoided because of increasing access time. Distributed capacitance forms a time constant with this output resistance causing slow rise and fall times when the resistor is large, adding to the access time.

Virtually any voltage comparator or sense amplifier can be used. Since total time is the sum of all delays, the sense amplifier is most often the fastest available. ON Semiconductors comparators NE521 and NE522 are ideal in this application because of low input offset voltages and very fast response. Using these Schottky clamped comparators significantly reduces the total cycle time of the memory.

Design of the sense amplifier network depends upon the transducer used and the input characteristics of the sense amplifier. The significant specifications are given in Table 2.

Table 2. Important Sense Amplifier Parameters

DEVICE	V_{OS} (mV)	I_B (μA)	$V_{IN\ (MIN)}$ (mV)	SPEED (ns) (V_{IN}=100mV)	GAIN
521	10	40	15	12	5000
522	10	40	15	15	5000

Consideration must first be given to the differential input voltage requirements of the sense amplifier. The required reference voltage is calculated from the relationship:

$$V_{REF} \leq (I_T - I_B)\ R1 - V_{DIFF}$$

Where I_T is the transducer output current, I_B is sense amplifier bias current and V_{DIFF} is minimum differential voltage to switch the sense amplifier.

In large systems, noise coupled into the sense lines by stray capacitance can be very troublesome. Judicious layout patterns with sense lines as short as possible will help, but will not always be sufficient. One method of eliminating noise is to use a balance sense line as shown in Figure 15.

A dummy line should be run parallel to the actual sense line in as close proximity as possible. One end is connected to the sense amplifier at the V_{REF} point while the other end is left open. The normal sense line is connected as usual. Electrical noise imposed upon the pair of sense lines takes the form of a common−mode signal and will be rejected by the sense amplifier. Signal currents in the sense line, on the other hand, form differential signals at the sense amp, causing the output to switch.

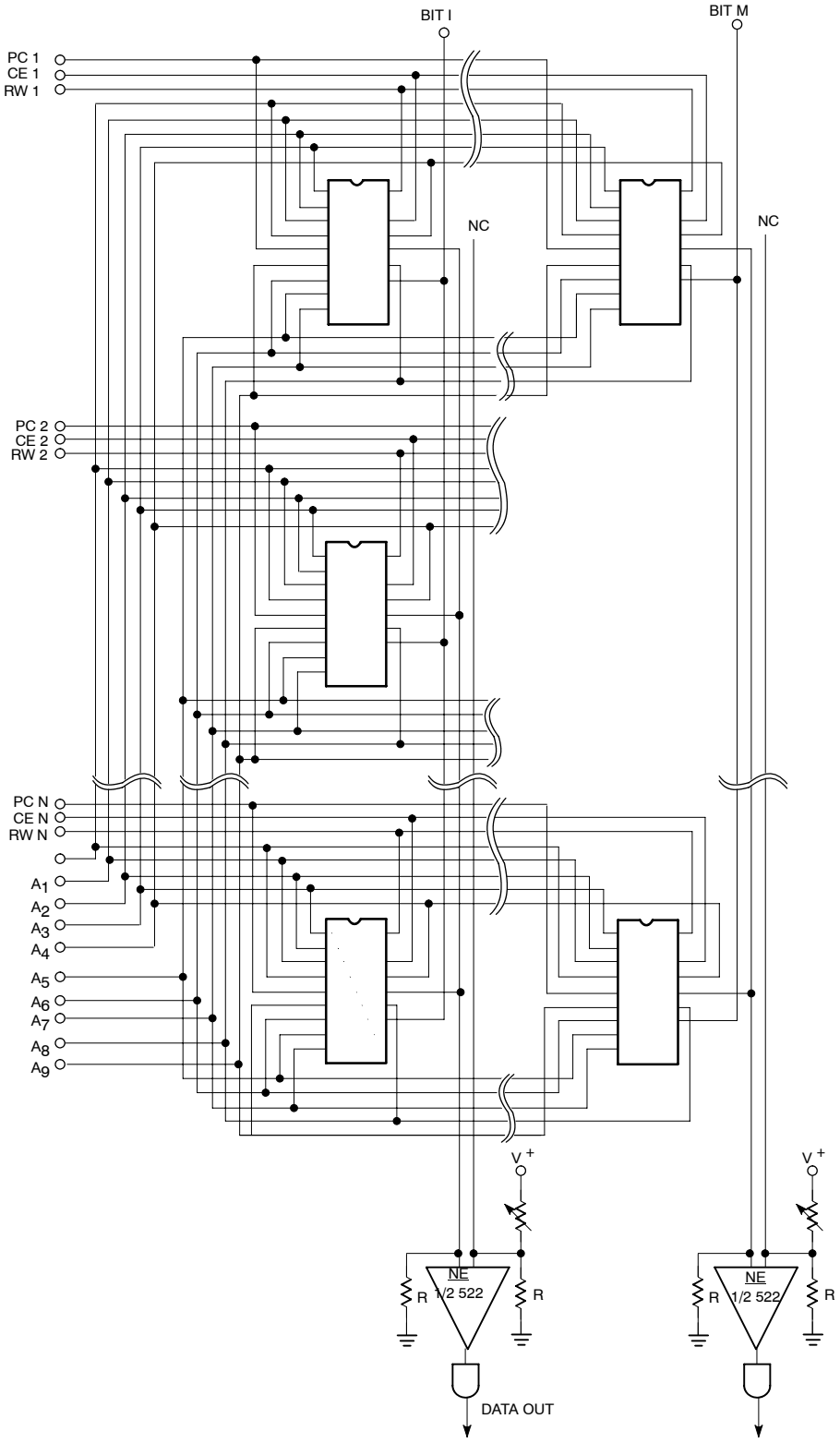


Figure 15. Balanced Sense Line to Reduce Noise

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